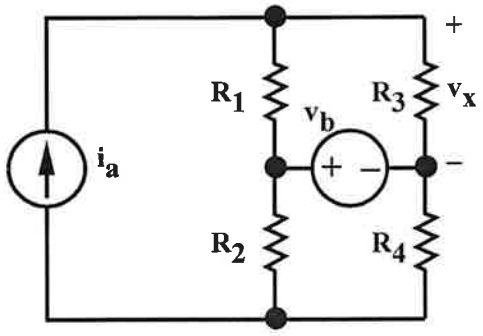
Problem P1: **Area Circuits I** **Student Code____**

Consider the following circuit in which
$i_a = 0.10$ A and
$v_b = 5.0 \sin(12t - \pi/2)$ V.
The resistor values are $R_1 = 50\ \Omega$, $R_2 = 25\ \Omega$, $R_3 = 50\ \Omega$, and $R_4 = 25\ \Omega$. The voltage $v_X(t)$ is across R_3.



(a) Using superposition principles, redraw the circuit showing only the contribution of i_a to the voltage v_X, i.e. v_{Xa}.

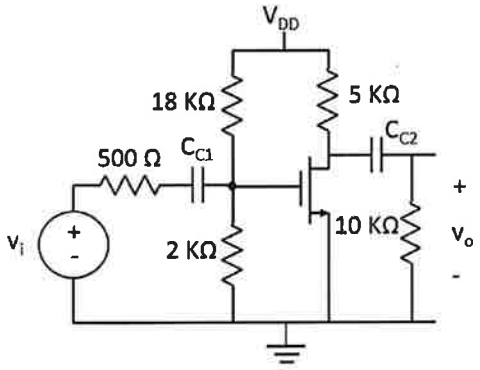
(b) Using superposition principles, redraw the circuit showing only the contribution of v_b to the voltage v_X, i.e. v_{Xb}.

(c) Using superposition, calculate the voltages v_{Xa}, v_{Xb}, and v_X.

(d) Calculate the RMS voltage $V_{X,RMS}$, i.e. the RMS value of v_X.

Problem 4: **Area: Circuits/Electronics** **Student Code____**

The parameters for the MOSFET in the common-source amplifier shown are: $g_m = 8\times10^{-2}\,A/V$ and $\lambda = 0$.



a) Draw the small-signal equivalent circuit with the C_{C_1} and C_{C_2} capacitors included.

b) Suppose we want to set the 3 dB frequency using C_{C_1}. Find the value of C_{C_1} to set the 3 dB frequency at 20 Hz.

Problem : P6 **Area: Communications / Signal Processing** **Student Code: _____**

Refer to Fig. 1 for the system with ideal Continuous-to-Discrete (C-to-D) and Discrete-to-Continuous (D-to-C) converters.

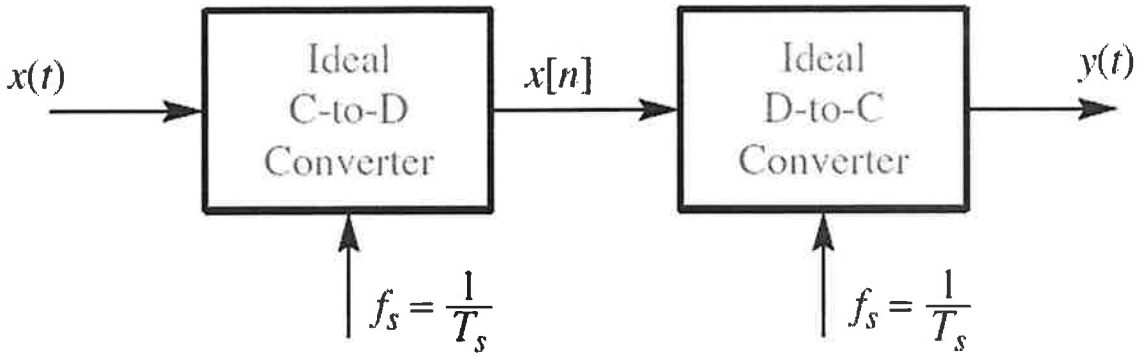


Figure 1: Ideal C-to-D and D-to-C system.

(a) Suppose that the output from the C-to-D converter is x[n] = cos(0.2πn), and the sampling rate of the C-to-D converter is f_s = 8000 samples/s. Determine a formula for the continuous-time sinusoidal input x(t) using the smallest frequency greater than 10000 Hz.

(b) Suppose the output from the C-to-D converter is x[n] = cos(0.25πn), the input signal is x(t) = cos(510πt), and the sampling rate (fs) of the C-to-D converter is less than 130 samples/s. Determine the largest possible sampling rate satisfying these three conditions.

Problem : P7 **Area: Communications / Signal Processing** **Student Code: ____**

Let a be a random variable which is uniformly distributed on the interval $[0,2]$. Define two random variables X and Y as

$$X \triangleq \min\{a, 2-a\},$$
$$Y \triangleq \max\{a, 2-a\},$$

and let $Z \triangleq \frac{Y}{X}$.

(1) Please derive the probability density function of X.

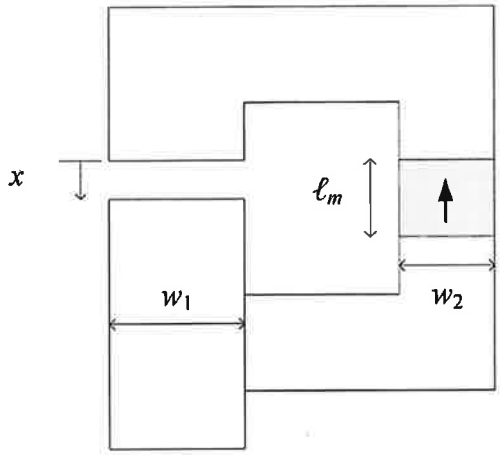
(2) Please derive the probability density function of Z.

(3) Please calculate the expectation of $\frac{X}{Y}$.

Problem: **P13** **Area** **Power** **Student Code____**

The device below is primarily composed of infinitely-permeable steel, with block of permanent magnet material indicated in gray and oriented as shown. The PM material has an equivalent coercivity of $H_c' = -950\ \mathrm{kA/m}$ and a recoil permeability of $\mu_R = 1.07\mu_0 = 1.345\times10^{-6}\ \mathrm{H/m}$.

Dimensions are: w_1 = 2 cm, w_2 = 1.25 cm, ℓ_m = 0.5 cm, depth into page 2 cm. The air gap length is variable, x.



a. Draw the magnetic equivalent circuit with the PM converted to a Thevenin equivalent. Label numerically.
b. Determine the flux linkage in the equivalent coil. At this point, you may have fictitious variables.
c. Determine the force acting to close the air gap. At this point, you may *not* have any fictitious variables. The only variable allowed is x.

Some useful equations:

$$\mathcal{R} = \frac{\ell}{\mu A}$$

$$(Ni)_{eq} = -H_c'\ell_m$$

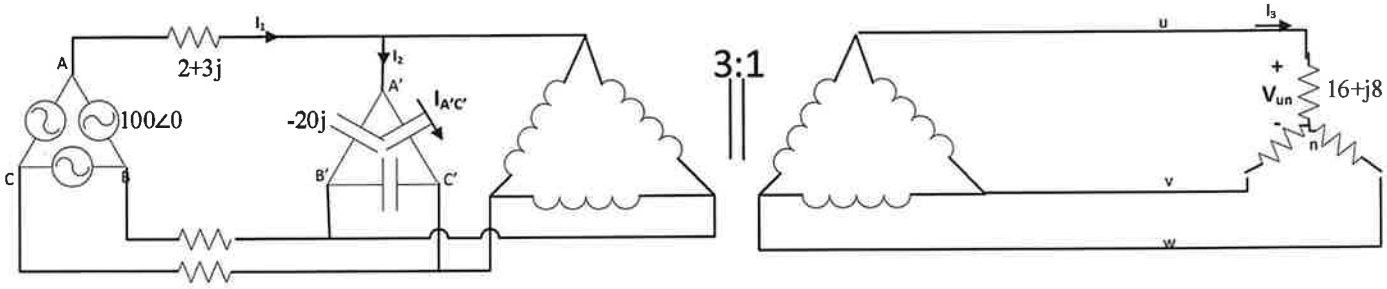
$$W_{fld}' = \int \lambda di$$

$$f_{fld} = \frac{\partial W_{fld}'}{\partial x}$$

Problem: P14 **Area: Power** **Student Code: _____**

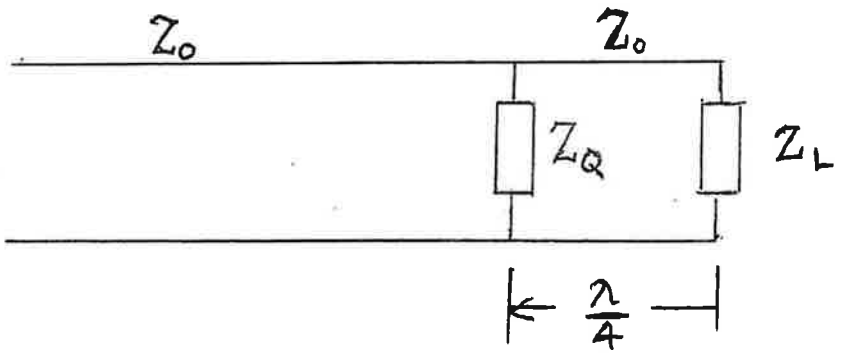
In the following circuit, find the following:

a) I_1, I_2, and I_3 (60 points).
b) $I_{A'C'}$ (Capacitor current) (10 points).
c) Phase voltage of the load (16+8j) equal to V_{un} (10 points).
d) 3-phase complex power of the source (20 points)



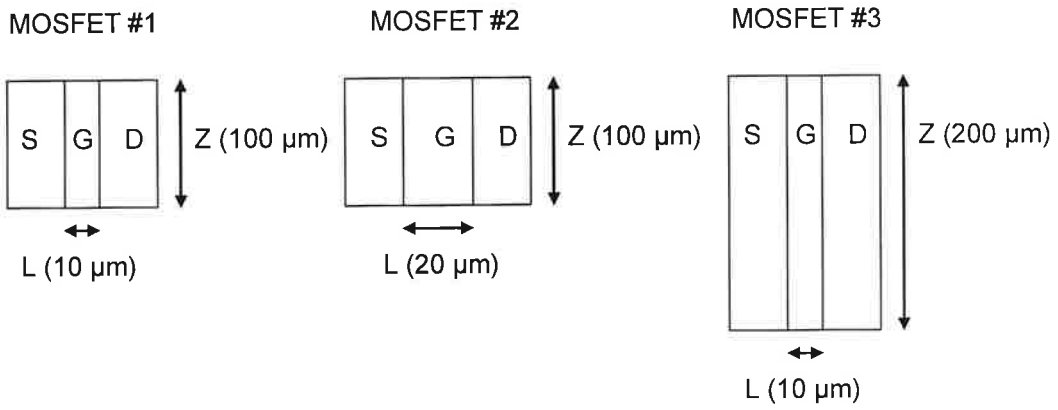
Qualifying Exam.

Problem # 18 :
A lossless transmission line of characteristic impedance, Z_o, is terminated with a load impedance, Z_L, whose value is half of the characteristic impedance. What impedance value of Z_Q should be used to put in parallel with the line $\lambda/4$ in front of the load to minimize the reflection?



Problem 19:_____ Area:_____Waves/Devices_____ Student Code:____

Three different MOSFET layouts are shown. For all three MOSFETs, the thickness (1.0 nm) and resistivity (1.0×10^{-3} Ωcm) of their inversion layers are uniform over the entire gate region.



< Figure. 1 Top View of Different MOSFETS >

a. Calculate the conductance of the inversion layer of each MOSFETs in Figure 1. (at $V_{DS} = 0$ V, i.e. the inversion layer thickness does not change).

b. If the drain-source current I_{DS} of MOSFET #1 is 10 mA at a given operational conditions (e.g. drain-source voltage V_{DS} and a gate-source voltage V_{GS}, etc.), calculate I_{DS} of #2 and #3 MOSFETs at the same conditions.

Constants*	Equations (p-type substrate MOSFET)*
$kT = 0.0259$ [eV] (at 300 K)	$\Psi_{s(inv)} = 2\Psi_B = (2kT / q) \ln(p_{po} / n_i)$
Si Bandgap = 1.12 [eV] (at 300 K)	$W_m = \sqrt{(2\varepsilon_s \Psi_{s(inv)} / qN_A)}$
Intrinsic carrier concentration of Silicon = 1×10^{10} [cm^{-3}] (at 300 K)	$V_T = V_o + \Psi_{s(inv)}$
$N_c = 2.86\times10^{19}$ [cm^{-3}] (at 300 K)	$V_T = qN_A W_m / C_o + \Psi_{s(inv)} = \sqrt{(2\varepsilon_s qN_A \Psi_{s(inv)})} / C_o + \Psi_{s(inv)}$
$N_v = 2.66\times10^{19}$ [cm^{-3}] (at 300 K)	$V_{FB} = \varphi_{ms} - (Q_f + Q_m + Q_{ot}) / C_o$
Elementary charge = 1.6×10^{-19} [C]	$R = \rho L / A$
$\varepsilon_o = 8.85E{-}14$ [F/cm]	$I_D = (Z / L)\mu_n C_o (V_G - V_T) V_D$ (when $V_D < V_G - V_T$)
$\varepsilon_s = 11.9\ \varepsilon_o$ [F/cm] (Si)	$I_D = (Z / 2L)\mu_n C_o (V_G - V_T)^2$ (when $V_D \geq V_G - V_T$)

$\varepsilon_{ox} = 3.9\ \varepsilon_o$ [F/cm]	(SiO_2)	

* Definition of parameters are not provided. It is expected that the examinee interprets the meaning.

Problem : 21 Area: Computational Intelligence **Student Code:**_____

Answer the follow questions.

a) When applying CI techniques to a given dataset, the dataset is broken up into training, cross-validation, and test sets. Define the terms data augmentation and data set imbalance as related to the training, cross-validation, and test partitioning of the dataset.

b) Describe the process of applying a CI technique to a training dataset to determine the parameters used in the CI technique. What are indicators that the parameters have been reasonably determined?

Problem : 22 Area: Computational Intelligence **Student Code:**_____

Answer the following questions.

(a) Define supervised and unsupervised learning. Give an example of a computational intelligence technique applied to supervised learning and an example of a computational intelligence technique applied to an unsupervised learning.

(b) Describe criteria that would be used to select a computational intelligence technique for analysis of a data set.

Problem : 23 Area: Computational Intelligence **Student Code:**_____

Answer the questions below.

Define the following terms:

(i) Clustering. Give two examples of clustering techniques.

(ii) Data mining. Give an example of an application where data mining is applied and how data mining is used.

(iii) Data fusion. Give two examples of applications where data fusion could be applied.

Problem : 24 Area: Computational Intelligence **Student Code:**_____

Describe the concept of General Disjunction Decomposition (GDD) for Evolvable Hardware. Provide diagrams and tables where necessary.

Embedded Systems

Problem1:

Assume that a particular processor is connected to external data memory as shown in Figure 1. In addition to the address and control lines seen in the figure, assume that the data lines of the external memory devices have been appropriately connected to the data bus of the processor.

(a) What is the address range for RAM2? Briefly justify your answer.

(b) Suppose that a hypothetical instruction, READX, is used to read the contents of external memory location B652H into the accumulator. From which RAM device will this byte be read? Briefly justify your answer.

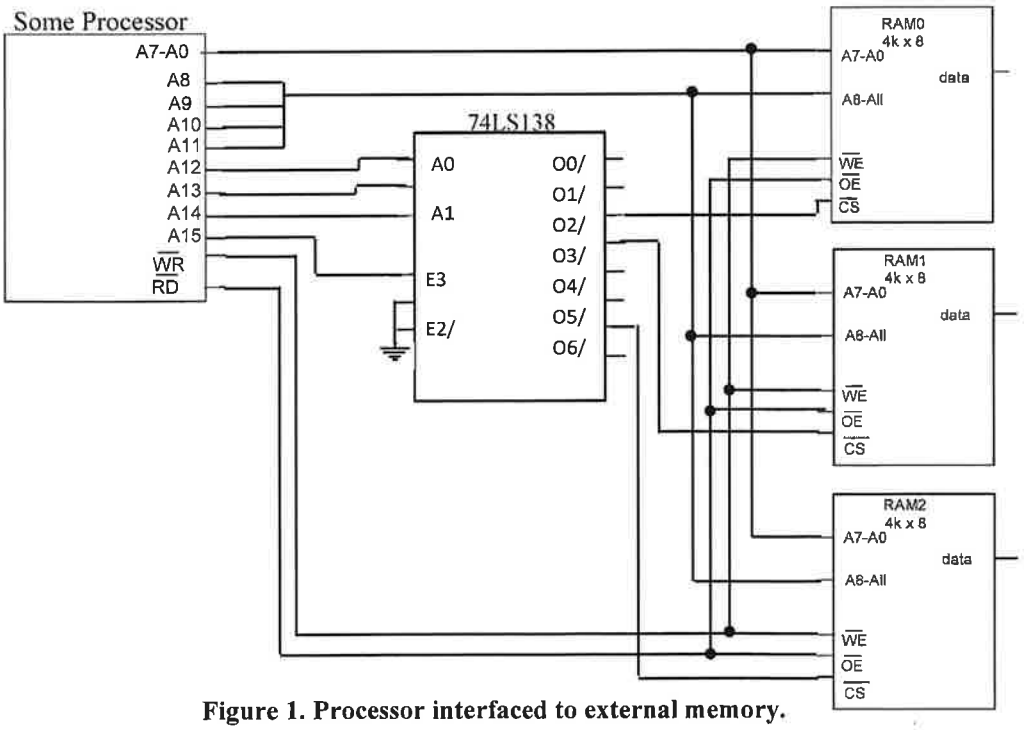


Figure 1. Processor interfaced to external memory.

Problem2:

Answer the questions for parts a and b below.

Interrupt processing in a microprocessor. These questions are not about a specific microprocessor but are about microprocessors in general.

(a) If you are asked to write some software for a microprocessor that uses an interrupt, what steps are required to properly setup a microprocessor so that the microprocessor can service the interrupt?

(b) In a typical microprocessor, when an interrupt condition occurs, a flag is set to indicate that condition to the microprocessor. Describe all the steps that occur after the flag is set and continuing until the microprocessor returns back to where it was in the main program. What is one thing the interrupt service routine must do?

Computer Architecture (choose any 2 problems)

Problem1:

Suppose you are trying to design an N-stage pipelined scalar processor. If branches cause 4 stall clock cycles with time fraction of 13%, loads cause 1 stall clock cycle with time fraction of 25% and the other instructions do not cause stalls, how many pipeline stages (i.e., N) are needed to achieve 5x speedup? Calculate the minimum N. (Hint: N should be greater than 5. So, try N = 6, 7,… and find the minimum N that can achieve 5x speedup.)

Problem2:

An ideal memory subsystem has the following requirements:

a) Infinite (in practice, high) capacity
b) Infinite (in practice, high) bandwidth
c) Instantaneous or zero (in practice, low) latency (access time)
d) Persistence or non-volatility
e) Zero to low implementation cost

Within the scope of the computer architecture course, describe one solution for meeting each requirement, and give a clear and detailed explanation of how the solution leads to the requirement being met.

Problem3:

a) Name and discuss three shortcomings of the scalar (uniprocessor) architecture.

b) Articulate one solution for each shortcoming as identified in part (a).

Problem : 29 Area: Integrated Circuits and Logic Design **Student Code:**_____

Answer the follow questions.

a) Using OR-gates and/or NOR-gates along with a 3-to-8 decoder, implement the function $f(a, b, c) = \sum m(0,2,4,7)$

b) Implement the function $f(a, b, c, d) = \prod M(0,1,3,6,9,12,15)$ using an 8:1 multiplexer and inverters.

Problem : 30 Area: Integrated Circuits and Logic Design **Student Code:**_____

Answer the questions for parts **a** and **b** below.

a. Simplify the logic expression F(x,y,z) = (x'+y')(y'+z')(x'+z)z' to obtain a logic expression that uses as few gates as possible (exclude inverters from the total gate count). Note that x' denotes NOT x. You may use any appropriate method for the logic simplification.

b. Construct the truth table for F(x,y,z) = (x'+y')(y'+z')(x'+z)z'.

Problem : 31 Area: Integrated Circuits and Logic Design **Student Code:**_____

Given the function: $F(w,x,y,z) = \sum(0,1,2,3,5,7,9,13)+dc(4,10,12)$

Answer the following questions.

a) Write the minimal sum-of-product expression for F.

wx \ yz	00	01	11	10
00				
01				
11				
10				

b) Write the minimal product-of-sums expression for F.

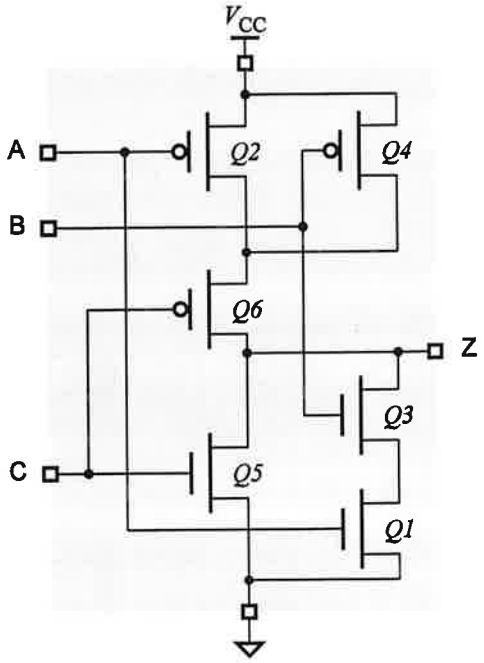
wx \ yz	00	01	11	10
00				
01				
11				
10				

c) Draw the simplified minimal product-of-sums expression for F from part b.

Problem : 32 Area: Integrated Circuits and Logic Design **Student Code:**_____

Answer the questions for parts **a** and **b** below.

a. For the CMOS circuit shown to the right, indicate whether each transistor is ON or OFF and the function output Z (H or L).



A	B	C	Q1	Q2	Q3	Q4	Q5	Q6	Z
L	L	L							
L	L	H							
L	H	L							
L	H	H							
H	L	L							
H	L	H							
H	H	L							
H	H	H							

b. Determine the logic function for Z from the CMOS logic circuit in part **a**.